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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte FREDERICK A. WARE and RICHARD E. PEREGO

Appeal 2015-003923
Application 12/482,626[1]
Technology Center 2100

Before MAHSHID D. SAADAT, NORMAN H. BEAMER, and MICHAEL J. ENGLE, *Administrative Patent Judges*.

ENGLE, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from a non-final rejection of claims 36–51, which are all of the claims pending in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

Technology

The application relates to "dynamic memory systems that perform overlapping refresh and data-access (read or write) transactions." Spec. Abstract.

Illustrative Claims

Claims 36 and 38 are illustrative and reproduced below with the limitations at issue emphasized:

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[1] Appellants state the real party in interest is Rambus Inc. App. Br. 2.

> 36. A discrete integrated circuit memory device comprising:
>
> a plurality of banks, each bank of the plurality of banks including an array of memory cells;
>
> *a command interface to receive commands from a controller device that is external to the discrete integrated circuit memory device at one or more pins of the discrete integrated circuit memory device*, the commands including a first command that specifies a refresh operation, and a second command that specifies a data transfer operation, wherein in response to the first command a first row of memory cells in a first bank is refreshed, and *while the first row of memory cells is being refreshed, the memory device accesses data from a second bank in response to the second command*; and
>
> an interface to transfer the data, accessed from the second bank, to the controller device.

> 38. The discrete integrated circuit memory device of claim 36, wherein the command interface receives the first command that specifies the refresh operation and the second command that specifies the date transfer operation as *a combined command*.

Rejections

Claims 36, 38, 39, 43, 44, 46, 47, and 51 stand rejected under 35 U.S.C. § 103(a) as obvious over the combination of Leung (US 6,449,685 B1; Sept. 10, 2002) and Deering et al. (US 6,195,106 B1; Feb. 27, 2001). Final Act. 3.

Claims 37, 41, 45, and 49 stand rejected under 35 U.S.C. § 103(a) as obvious over the combination of Leung, Deering, and Matsumoto et al. (US 2002/0191467 A1; Dec. 19, 2002). Final Act. 5.

Claims 40 and 48 stand rejected under 35 U.S.C. § 103(a) as obvious over the combination of Leung, Deering, and Funyu et al. (US 6,535,950 B1; Mar. 18, 2003). Final Act. 6.

Claims 42 and 50 stand rejected under 35 U.S.C. § 103(a) as obvious over the combination of Leung, Deering, and Koyanagi et al. (US 2002/0114209 A1; Aug. 22, 2002). Final Act. 7.

ISSUES

1. Did the Examiner err in finding the combination of Leung and Deering teaches or suggests "a command interface to receive commands from a controller device that is external to the discrete integrated circuit memory device at one or more pins of the discrete integrated circuit memory device" and "while the first row of memory cells is being refreshed, the memory device accesses data from a second bank in response to the second command," as recited in independent claim 36?

2. Did the Examiner err in finding Leung teaches or suggests "a combined command," as recited in dependent claim 38?

ANALYSIS

Claims 36, 37, 39–45, and 47–51

Independent claim 36 recites "a command interface to receive commands from a controller device that is external to the discrete integrated circuit memory device at one or more pins of the discrete integrated circuit memory device" and "while the first row of memory cells is being refreshed [in response to the first command], the memory device accesses data from a second bank in response to the second command."

Appellants contend neither Leung nor Deering teaches these limitations. App. Br. 10–11. Specifically, "Leung merely discloses write and read commands are received . . . from the external device, but Leung is silent with respect to the memory device receiving refresh commands from the external device . . . since the refresh commands in Leung are generated

internally within the memory device." *Id.* at 11 (emphasis omitted). However, regardless of what Leung teaches, the Examiner finds "Deering is relied upon to disclose . . . . an external controller for providing refresh operations to DRAM banks. Specifically, [Deering's] rendering controller 70 refreshes a page of the DRAM banks A-D." Ans. 8 (citing Deering 35:64–67, 36:9–17, 10:35–40, Figs. 1 & 29); *see also* Ans. 3–4. Thus, Deering teaches the limitations that Appellants argue are missing in Leung.

Similarly, Appellants argue "Deering discloses a rendering controller 70 that is external to the FBRAM chip" (App. Br. 6), but "nowhere in the cited section of Deering does it disclose that the memory is accessed in response to a data access command while the memory is being refreshed in response to a refresh command." Reply Br. 9. However, regardless of what Deering teaches, Appellants concede Leung discloses a memory with "DRAM banks that can operate independent of each other so that parallel operations, such as read, write and refresh, can take place in different DRAM banks simultaneously." App. Br. 6 (quoting Leung 6:45–48); *see also* Ans. 3 (citing Leung 3:44–49 ("the memory banks are independently controlled")), 10 ("Leung discloses the limitation of a command that specifies a data transfer operation.") (citing Leung 2:63–67). Thus, Leung teaches the limitations that Appellants argue are missing in Deering.

"Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Moreover, Appellants have not sufficiently persuaded us against the Examiner's findings regarding why a person of ordinary skill at the time of the invention would have been motivated to combine the analogous

DRAM devices of Leung and Deering, including "providing the benefit of enabling concurrent operation" and "to reduce electrical turn around delays for faster read/write." Ans. 4, 8, 10.

Appellants argue "Leung specifically teaches away from the use of an external memory controller" because Leung teaches a system with an internal controller. App. Br. 6–9. "A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (quotation omitted). Here, Appellants have not sufficiently identified any way in which Leung criticizes, discredits, or otherwise discourages an external controller.

For the same reasons, we are not persuaded by Appellants' argument that modifying Leung to have an external controller would change Leung's "principle of operation." App. Br. 9. Merely because there is a "difference" between two prior art references does not necessarily affect the "principle of operation." *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012).

Appellants further argue Matsumoto, Funyu, and Koyangai do "not cure the deficiencies of Leung and Deering." App. Br. 11–12. However, we are not persuaded Leung and Deering are deficient for the reasons above.

Accordingly, we sustain the Examiner's rejection of claim 36, and claims 37, 39–45, and 47–51, which Appellants argue are patentable for similar reasons. *See* App. Br. 7, 11–12; 37 C.F.R. § 41.37(c)(1)(iv).

Claims 38 and 46

Claim 38 recites "the command interface receives the first command that specifies the refresh operation and the second command that specifies

the date transfer operation as *a combined command*." Claim 46 recites a commensurate limitation.

The Examiner relies on Leung for this limitation. Ans. 10–11; Non-Final Act. 4. "According to broadest reasonable interpretation of claimed 'combined,' commands are combined when they trigger a performance in parallel and/or simultaneous processing." Ans. 11. In Leung, "[t]he refresh is triggered when an access command is received, thus combining the operations which are triggered by one command (read or write), thus disclosing a combined command." *Id.*

However, we agree with Appellants that "[i]t is not 'reasonable' to interpret a claim limitation that specifically recites that the first and second commands must be *received* together as a combined command to . . . focus[] on when the commands are *processed*" rather than when they are *received*. Reply Br. 13 (emphasis added, original emphasis omitted).

Accordingly, we do not sustain the rejection of claims 38 and 46.

DECISION

For the reasons above, we affirm the Examiner's decision rejecting claims 36, 37, 39–45, and 47–51.

We reverse the Examiner's decision rejecting claims 38 and 46.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

AFFIRMED-IN-PART